LM7705 Low Noise Negative Bias Generator

Check for Samples: LM7705

FEATURES

- **Regulated Output Voltage −0.232V**
- **Output Voltage Tolerance 5%**
- **Output Voltage Ripple 4 mV$_{PP}$**
- **Max Output Current 26 mA**
- **Supply Voltage 3V to 5.25V**
- **Conversion Efficiency up to 98%**
- **Quiescent Current 78 µA**
- **Shutdown Current 20 nA**
- **Turn on Time 500 µs**
- **Operating Temperature Range −40°C to 125°C**
- **8-Pin VSSOP Package**

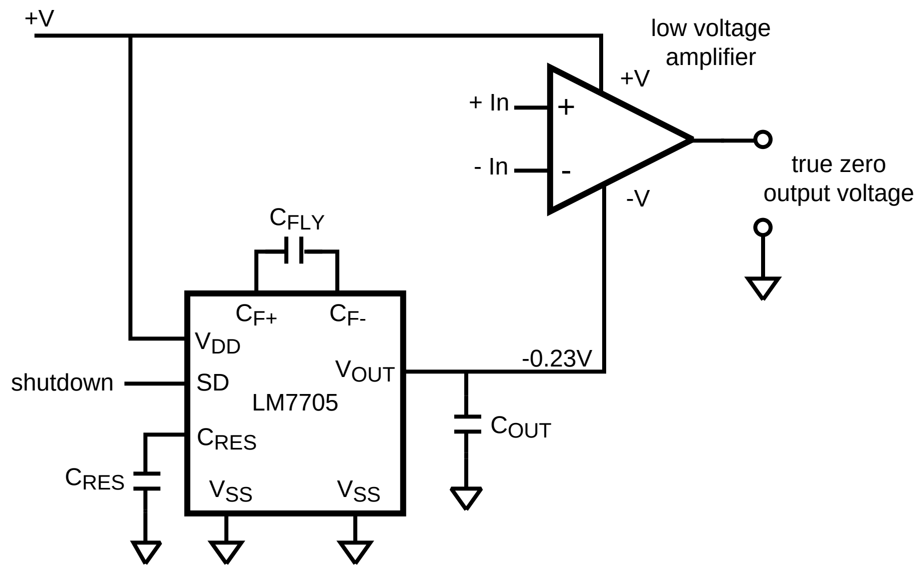
APPLICATIONS

- **True Zero Amplifier Output**
- **Portable Instrumentation**
- **Low Voltage Split Power Supplies**

DESCRIPTION

The LM7705 is a switched capacitor voltage inverter with a low noise, −0.23V fixed negative voltage regulator. This device is designed to be used with low voltage amplifiers to enable the amplifiers output to swing to zero volts. The −0.23 volts is used to supply the negative supply pin of an amplifier while maintaining less then 5.5 volts across the amplifier. Rail-to-Rail output amplifiers cannot output zero volts when operating from a single supply voltage and can result in error accumulation due to amplifier output saturation voltage being amplified by following gain stages. A small negative supply voltage will prevent the amplifiers output from saturating at zero volts and will help maintain an accurate zero through a signal processing chain. Additionally, when an amplifier is used to drive an ADC's input, it can output a zero voltage signal and the full input range of an ADC can be used. The LM7705 has a shutdown pin to minimize standby power consumption

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[1][2]

			VALUE
Supply Voltage V_{DD} - V_{SS}			+5.75V
SD			V_{DD}+0.3V, V_{SS}-0.3V
ESD Tolerance[3]	Human Body Model	For input pins only	2000V
		For all other pins	2000V
	Machine Model		200V
	Charged Device Model		750V
Storage Temp. Range			−65°C to 150°C
Junction Temperature[4]			150°C max
Mounting Temperature	Infrared or Convection (20 sec)		260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine model, applicable std JESD22–A115–A (ESSD MM srd of JEDEC). Field induced Charge-Device Model, applicable std. JESD22–C101–C. (ESD FICDM std of JEDEC).
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

Operating Ratings

Supply Voltage (V_{DD} to GND)		3V to 5.25V
Supply Voltage (V_{DD} wrt V_{OUT})		3.23V to 5.48V
Temperature Range		−40°C to 125°C
Thermal Resistance (θ_{JA})	8-Pin VSSOP	253°C/W

3.3V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_{DD} = 3.3V, V_{SS} = 0V, SD = 0V, C_{FLY}= 5 µF, C_{RES} = 22 µF, C_{OUT} = 22 µF. **Boldface** limits apply at temperature extremes (1).

Symbol	Parameter	Conditions	Min[2]	Typical[3]	Max[2]	Units
V_{OUT}	Output Voltage	I_{OUT} = 0 mA	−0.242 **−0.251**	−0.232	−0.219 **−0.209**	V
		I_{OUT} = −20 mA	−0.242 **−0.251**	−0.226	−0.219 **−0.209**	
V_R	Output Voltage Ripple	I_{OUT} = −20 mA		4		mV_{PP}
I_S	Supply Current	No Load	50	78	100 **150**	µA
I_{SD}	Shutdown Supply Current	SD = V_{DD}		20		nA
η_{POWER}	Current Conversion Efficiency	−5 mA ≤ I_{OUT} ≤ −20 mA		98		%
η_{POWER}	Current Conversion Efficiency	I_{OUT} = −5 mA		98		%
t_{ON}	Turn On Time	I_{OUT} = −5 mA		500		µs
t_{OFF}	Turn Off Time	I_{OUT} = −5 mA		700		µs
$t_{OFF\ CP}$	Turn Off Time Charge Pump	I_{OUT} = −5 mA		11		µs
Z_{OUT}	Output Impedance	−1 mA ≤ I_{OUT} ≤ −20 mA		0.23	0.8 **1.3**	Ω
I_{O_MAX}	Maximum Output Current	V_{OUT} < −200 mV	-26			mA
f_{OSC}	Oscillator Frequency			92		kHz

(1) Boldface limits apply to temperature range of −40°C to 125°C
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

3.3V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_{DD} = 3.3V, V_{SS} = 0V, SD = 0V, C_{FLY}= 5 µF, C_{RES} = 22 µF, C_{OUT} = 22 µF. **Boldface** limits apply at temperature extremes (1).

Symbol	Parameter	Conditions	Min(2)	Typical(3)	Max(2)	Units
V_{IL}	Shutdown Input Low				1.6 **1.25**	V
V_{IH}	Shutdown Input High		1.85 **2.15**			V
I_C	Shutdown Pin Input Current	SD = V_{DD}		50		pA
	Load Regulation	0 mA ≤ I_{OUT} ≤ −20 mA		0.12	0.6 **0.85**	%/mA
	Line Regulation	3V ≤ V_{DD} ≤ 5.25V (No Load)	-0.2	0.29	0.7 **1.1**	%/V

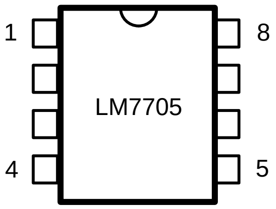
5.0V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V_{DD} = 5.0V, V_{SS} = 0V, SD = 0V, C_{FLY} = 5 µF, C_{RES} = 22 µF, C_{OUT} = 22 µF. **Boldface** limits apply at temperature extremes (1).

Symbol	Parameter	Conditions	Min(2)	Typical(3)	Max(2)	Units
V_{OUT}	Output Voltage	I_{OUT} = 0 mA	−0.242 **−0.251**	−0.233	−0.219 **−0.209**	V
		I_{OUT} = −20 mA	−0.242 **−0.251**	−0.226	−0.219 **−0.209**	
V_R	Output Voltage Ripple	I_{OUT} = −20 mA		4		mV_{PP}
I_S	Supply Current	No Load	60	103	135 **240**	µA
I_{SD}	Shutdown Supply Current	SD = V_{DD}		20		nA
η_{POWER}	Current Conversion Efficiency	−5 mA ≤ I_{OUT} ≤ −20 mA		98		%
η_{POWER}	Current Conversion Efficiency	I_{OUT} = −5 mA		98		%
t_{ON}	Turn On Time	I_{OUT} = −5 mA		200		µs
t_{OFF}	Turn Off Time	I_{OUT} = −5 mA		700		µs
$t_{OFF\ CP}$	Turn Off Time Charge Pump	I_{OUT} = −5 mA		11		µs
Z_{OUT}	Output Impedance	−1 mA ≤ I_{OUT} ≤ −20 mA		0.26	0.8 **1.3**	Ω
I_{O_MAX}	Maximum Output Current	V_{OUT} < − 200 mV	−35			mA
f_{OSC}	Oscillator Frequency			91		kHz
V_{IL}	Shutdown Input Low				2.55 **1.95**	V
V_{IH}	Shutdown Input High		2.8 **3.25**			V
I_C	Shutdown Pin Input Current	SD = V_{DD}		50		pA
	Load Regulation	0 mA ≤ I_{OUT} ≤ −20 mA		0.14	0.6 **0.85**	%/mA
	Line Regulation	3V ≤ V_{DD} ≤ 5.25V (No Load)	−0.2	0.29	0.7 **1.1**	%/V

(1) Boldface limits apply to temperature range of −40°C to 125°C
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

Connection Diagram

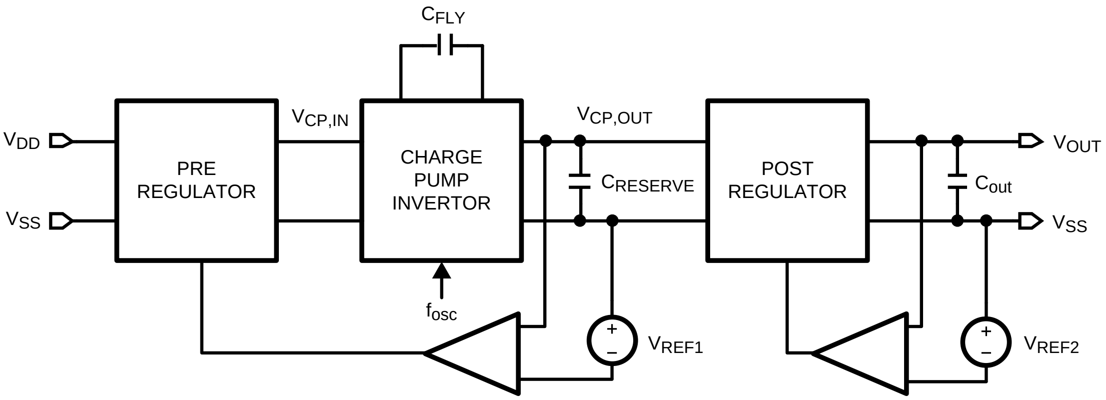


8-Pin VSSOP -Top View

PIN DESCRIPTIONS

Pin Number	Symbol	Description
1	C_{F+}	C_{FLY} Positive Capacitor Connection
2	V_{SS}	Power Ground
3	SD	Shutdown Pin If SD pin is LOW, device is ON If SD pin is HIGH, device is OFF
4	V_{DD}	Positive Supply Voltage
5	V_{SS}	Power Ground
6	V_{OUT}	Output Voltage
7	C_{RES}	Reserve Capacitor Connection
8	C_{F-}	C_{FLY} Negative Capacitor Connection

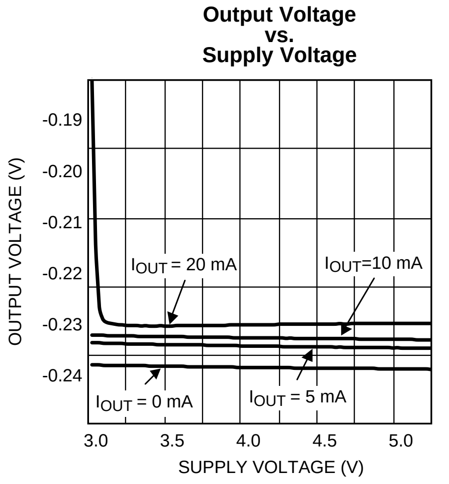
Block Diagram



LM7705

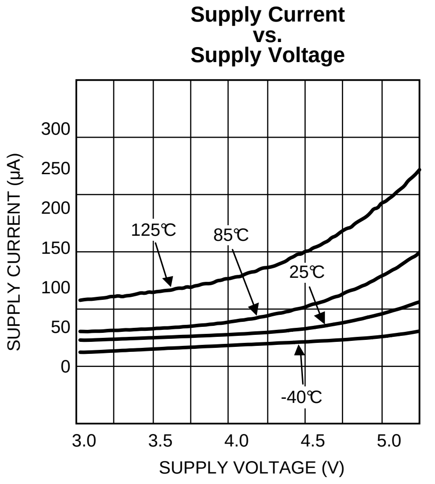
Typical Performance Characteristics

V_{DD} = 3.3V and T_A = 25°C unless otherwise noted.



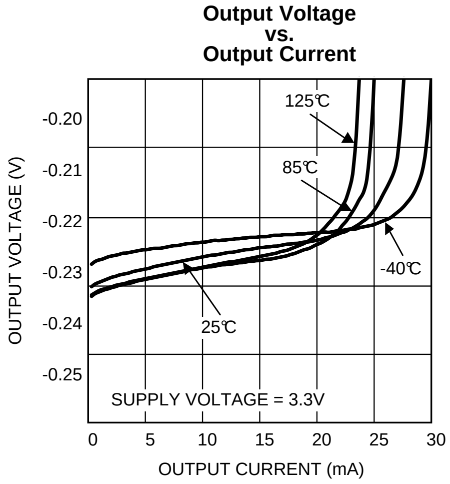
Output Voltage vs. Supply Voltage

Figure 1.



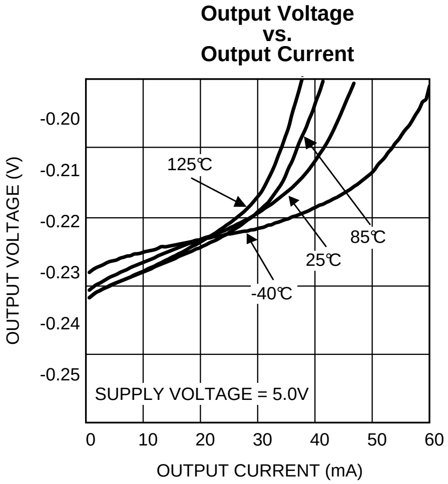
Supply Current vs. Supply Voltage

Figure 2.



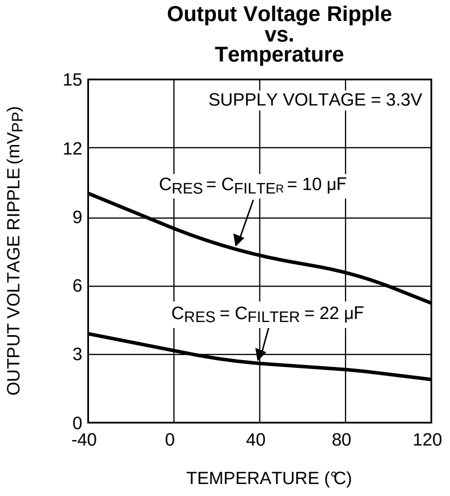
Output Voltage vs. Output Current

Figure 3.



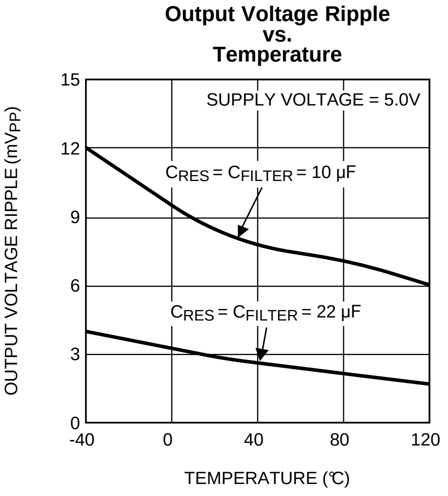
Output Voltage vs. Output Current

Figure 4.



Output Voltage Ripple vs. Temperature

Figure 5.



Output Voltage Ripple vs. Temperature

Figure 6.

Typical Performance Characteristics (continued)

V_{DD} = 3.3V and T_A = 25°C unless otherwise noted.

Supply Current vs. Output Current

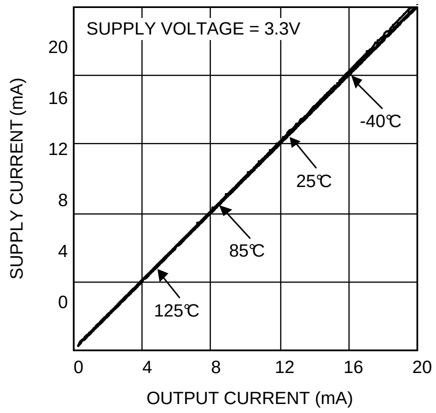


Figure 7.

Supply Current vs. Output Current

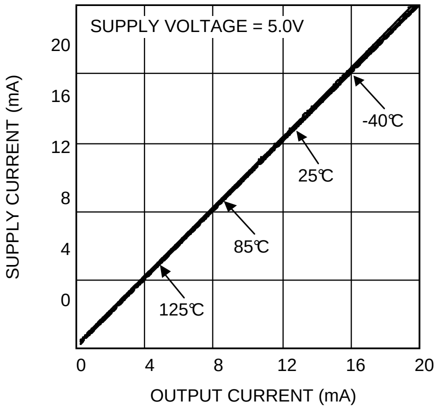


Figure 8.

Current Conversion Efficiency vs. Output Current

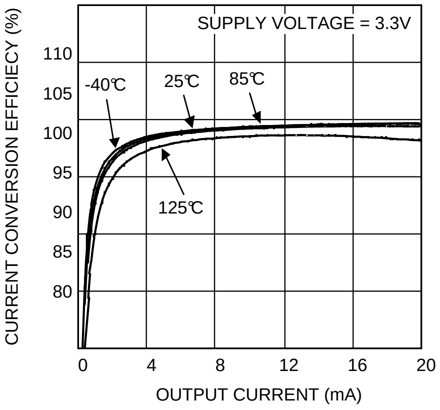


Figure 9.

Current Conversion Efficiency vs. Output Current

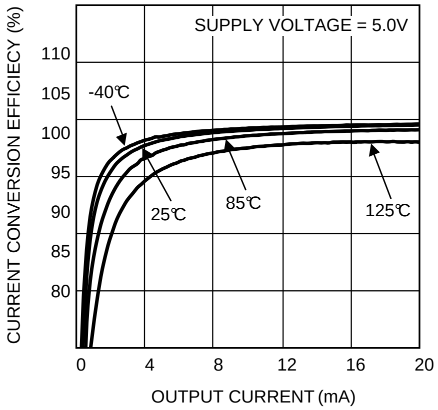


Figure 10.

Turn On Time

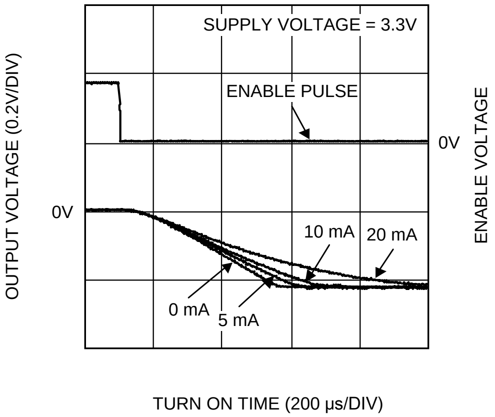


Figure 11.

Turn On Time

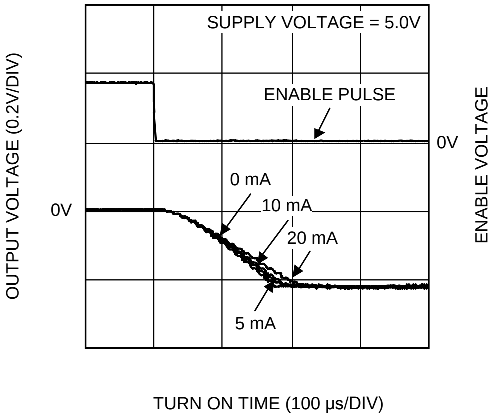


Figure 12.

Typical Performance Characteristics (continued)

V_{DD} = 3.3V and T_A = 25°C unless otherwise noted.

Load Regulation vs. Temperature

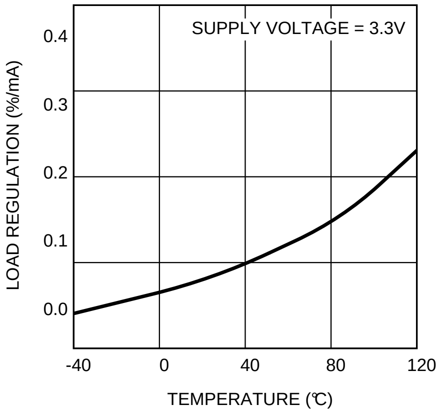


Figure 13.

Load Regulation vs. Temperature

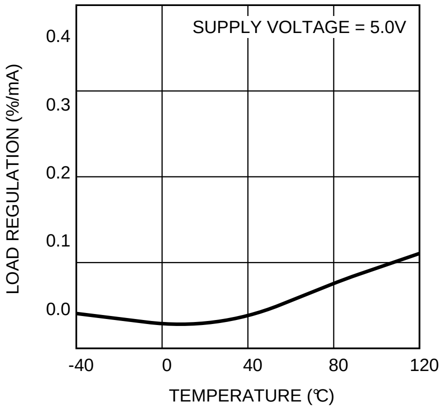


Figure 14.

Transient Response

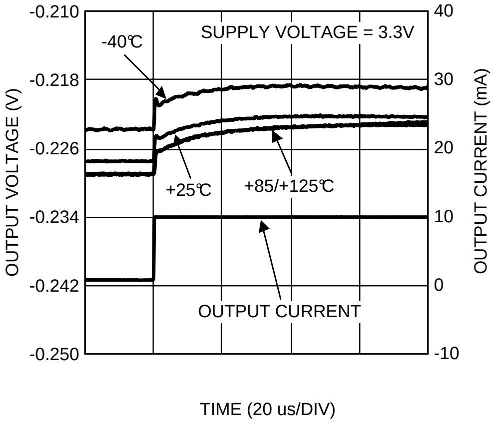


Figure 15.

Transient Response

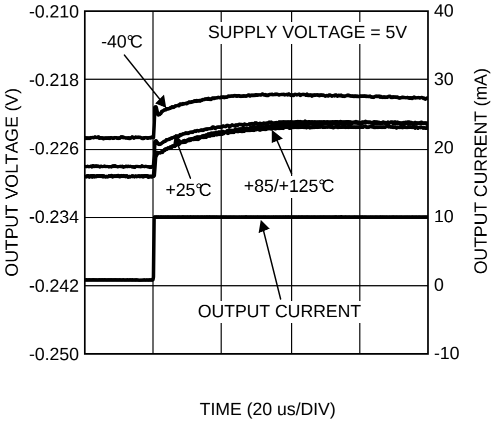


Figure 16.

Transient Response

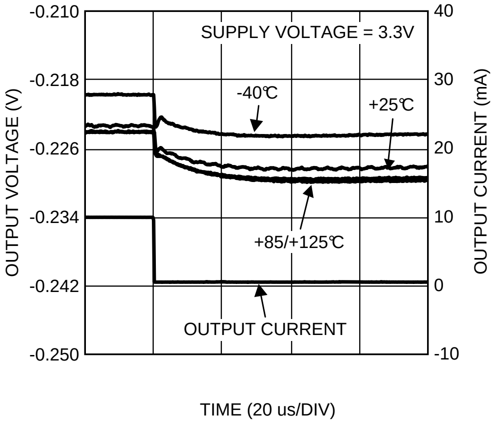


Figure 17.

Transient Response

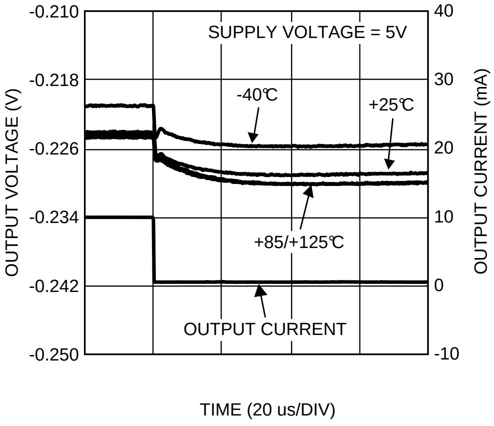


Figure 18.

Typical Performance Characteristics (continued)

V_{DD} = 3.3V and T_A = 25°C unless otherwise noted.

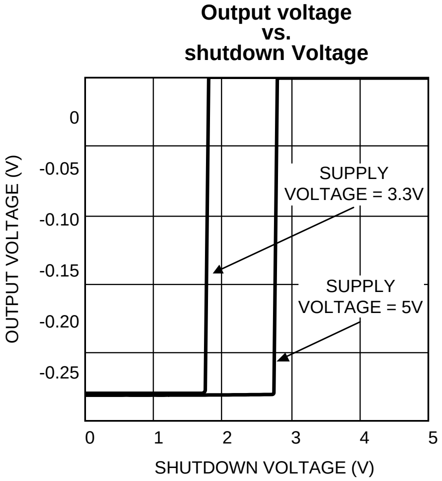


Figure 19.

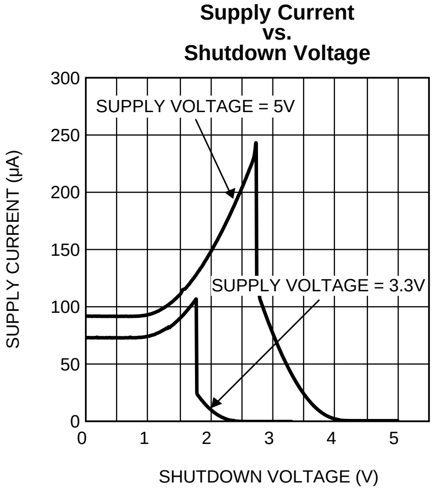


Figure 20.

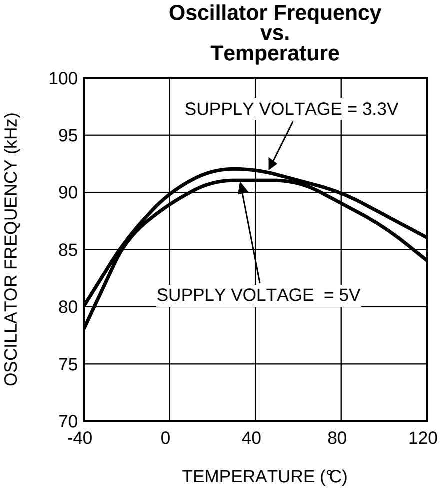


Figure 21.

APPLICATION INFORMATION

This applications section will give a description of the functionality of the LM7705. The LM7705 is a switched capacitor voltage inverter with a low noise, −0.23V fixed negative bias output. The part will operate over a supply voltage range of 3 to 5.25 Volt. Applying a logical low level to the SD input will activate the part, and generate a fixed −0.23V output voltage. The part can be disabled; the output is switched to ground level, by applying a logical high level to the SD input of the part.

FUNCTIONAL DESCRIPTION

The LM7705, low noise negative bias generator, can be used for many applications requiring a fixed negative voltage. A key application for the LM7705 is an amplifier with a true zero output voltage using the original parts, while not exceeding the maximum supply voltage ratings of the amplifier.

The voltage inversion in the LM7705 is achieved using a switched capacitor technique with two external capacitors (C_{FLY} and C_{RES}). An internal oscillator and a switching network transfers charge between the two storage capacitors. This switched capacitor technique is given in Figure 22.

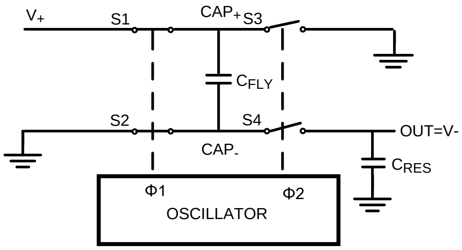


Figure 22. Voltage Inverter

The internal oscillator generates two anti-phase clock signals. Clock 1 controls switches S1 and S2. Clock 2 controls switches S3 and S4. When Switches S1 and S2 are closed, capacitor C_{FLY} is charged to V^+. When switches S3 and S4 are closed (S1 and S2 are open) charge from C_{FLY} is transferred to C_{RES} and the output voltage OUT is equal to $-V^+$.

Due to the switched capacitor technique a small ripple will be present at the output voltage, with a frequency of the oscillator. The magnitude of this ripple will increase for increasing output currents. The magnitude of the ripple can be influenced by changing the values of the used capacitors.

In the next section a more detailed technical description of the LM7705 will be given.

TECHNICAL DESCRIPTION

As indicated in the functional description section, the main function of the LM7705 is to supply a stabilized negative bias voltage to a load, using only a positive supply voltage. A general block diagram for this charge pump inverter is given in Figure 23. The external power supply and load are added in this diagram as well.

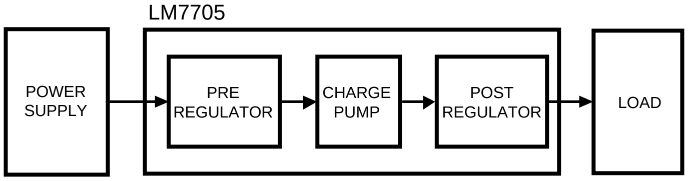


Figure 23. LM7705 Architecture

The architecture given in Figure 23 shows that the LM7705 contains 3 functional blocks:

- Pre-regulator
- Charge pump inverter
- Post-regulator

The output voltage is stabilized by:

- Controlling the power supplied from the power supply to the charge pump input by the pre-regulator
- The power supplied from the charge pump output to the load by the post-regulator.

A more detailed block diagram of the negative bias generator is given in Figure 24. The control of the pre-regulator is based on measuring the output voltage of the charge pump. The goal of the post-regulator is to provide an accurate controlled negative voltage at the output, and acts as a low pass filter to attenuate the output voltage ripple. The voltage ripple is a result of the switching behavior of the charge pump and is dependent of the output current and the values of the used capacitors.

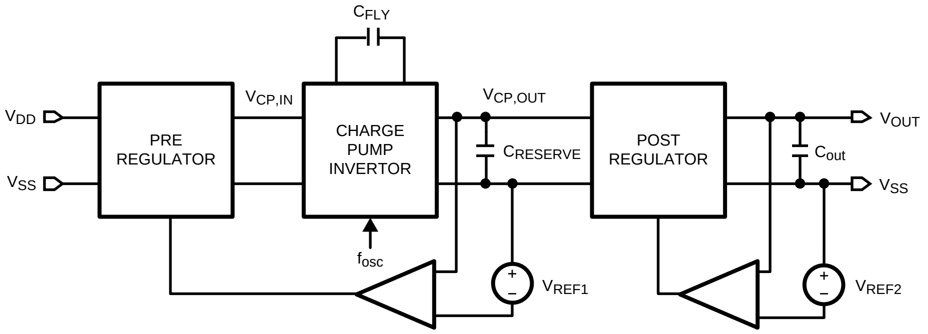


Figure 24. Charge Pump Inverter with Input/Output Control

In the next section a simple equation will be derived, that shows the relation between the ripple of the output current, the frequency of the internal clock generator and the value of the capacitor placed at the output of the LM7705.

Charge Pump Theory

This section uses a simplified but realistic equivalent circuit that represents the basic function of the charge pump. The schematic is given in Figure 25.

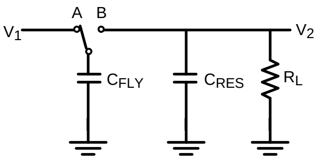


Figure 25. Charge Pump

When the switch is in position A, capacitor C_{FLY} will charge to voltage V_1. The total charge on capacitor C_{FLY} is $Q_1 = C_{FLY} \times V_1$. The switch then moves to position B, discharging C_{FLY} to voltage V_2. After this discharge, the charge on C_{FLY} will be $Q_2 = C_{FLY} \times V_2$. Note that the charge has been transferred from the source V_1 to the output V_2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C_{FLY}(V1 - V2) \tag{1}$$

When the switch changes between A and B at a frequency f, the charge transfer per unit time, or current is:

$$I = f\,\Delta q = f\,C_{FLY}(V1 - V2) \tag{2}$$

The switched capacitor network can be replaced by an equivalent resistor, as indicated in Figure 26.

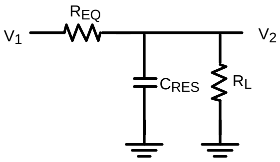


Figure 26. Switched Capacitor Equivalent Circuit

The value of this resistor is dependent on both the capacitor value and the switching frequency as given in Equation 3

$$I = \frac{V1 - V2}{\left(\frac{1}{f\,C_{FLY}}\right)} = \frac{V1 - V2}{R_{EQ}} \tag{3}$$

The value for R_{EQ} can be calculated from Equation 3 and is given in Equation 4

$$R_{EQ} = \left(\frac{1}{f\,C_{FLY}}\right) \tag{4}$$

Equation 4 show that the value for the resistance at an increased internal switching frequency, allows a lower value for the used capacitor.

Key Specification

The key specifications for the LM7705 are given in the following overview:

Supply Voltage	The LM7705 will operate over a supply voltage range of 3V to 5.25V, and meet the specifications given in the Electrical Table. Supply voltage lower than 3.3 Volt will decrease performance (The output voltage will shift towards zero, and the current sink capabilities will decrease) A voltage higher than 5.25V will exceed the Abs Max ratings and therefore damage the part.
Output Voltage/Line Regulation	The fixed and regulated output voltage of −0.23 V has tight limits, as indicated in the Electrical Characteristics table, to ensure a stable voltage level. The usage of the pre- and post regulator in combination with the charge pump inverter ensures good line regulation of 0.29%/V
Output current/Load regulation	The LM7705 can sink currents > 26 mA, causing an output voltage shift to −200 mV. A specified load-regulation of 0.14% mA/V ensures a minor voltage deviation for load current up to 20 mA.
Quiescent current	The LM7705 consumes a quiescent current less than 100 µA. Sinking a load current, will result in a current conversion efficiency better than 90%, even for load currents of 1 mA, increasing to 98% for a current of 5mA.

In the next section a general amplifier application requiring a true-zero output, will be discussed, showing an increased performance using the LM7705.

GENERAL AMPLIFIER APPLICATION

This section will discuss a general DC coupled amplifier application. First, one of the limitations of a DC coupled amplifier is discussed. This is illustrated with two application examples. A solution is a given for solving this limitation by using the LM7705.

Due to the architecture of the output stage of general amplifiers, the output transistors will saturate. As a result, the output of a general purpose op amp can only swing to a few 100 mV of the supply rails. Amplifiers using CMOS technology do have a lower output saturation voltage. This is illustrated in Figure 27. E.g. Texas Instruments' LM7332 can swing to 200 mV to the negative rail, for a 10 kΩ load, over all temperatures.

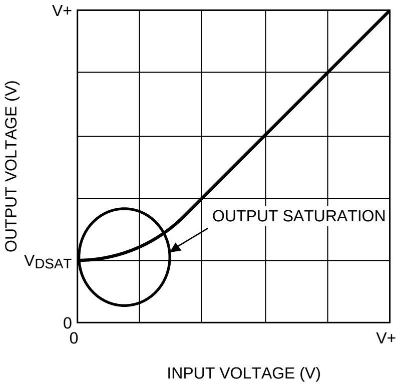


Figure 27. Limitation of the Output of an Amplifier

The introduction of operational amplifiers with output Rail-to-rail drive capabilities is a strong improvement and the (output) performance of op amps is for many applications no longer a limiting factor. For example, Texas Instruments' LMP7701 (a typical rail-to-rail op amp), has an output drive capability of only 50 mV over all temperatures for a 10 kΩ load resistance. This is close to the lower supply voltage rail.

However, for true zero output applications with a single supply, the saturation voltage of the output stage is still a limiting factor. This limitation has a negative impact on the functionality of true zero output applications. This is illustrated in Figure 28.

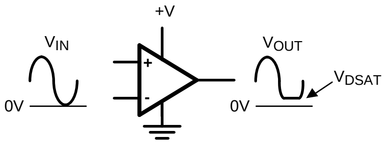


Figure 28. Output Limitation for Single Supply True Zero Output Aapplication

In the following section, two applications will be discussed, showing the limitations of the output stage of an op amp in a single supply configuration.

- A single stage true zero amplifier, with a 12 bit ADC back end.
- A dual stage true zero amplifier, with a 12 bit ADC back end.

One-stage, Single Supply True Zero Amplifier

This application shows a sensor with a DC output signal, amplified by a single supply op amp. The output voltage of the op amp is converted to the digital domain using an Analog to Digital Converter (ADC). Figure 29 shows the basic setup of this application.

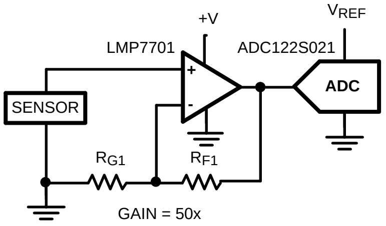


Figure 29. Sensor with DC Output and a Single Supply Op Amp

The sensor has a DC output signal that is amplified by the op amp. For an optimal signal-to-noise ratio, the output voltage swing of the op amp should be matched to the input voltage range of the Analog to Digital Converter (ADC). For the high side of the range this can be done by adjusting the gain of the op amp. However, the low side of the range can't be adjusted and is affected by the output swing of the op amp.

Example:

Assume the output voltage range of the sensor is 0 to 90 mV. The available op amp is a LMP7701, using a 0/+5V supply voltage, having an output drive of 50 mV from both rails. This results in an output range of 50 mV to 4.95V.

Let choose two resistors values for R_{G1} and R_{F1} that result in a gain of 50x. The output of the LMP7701 should swing from 0 mV to 4.5V. The higher value is no problem, however the lower swing is limited by the output of the LM7701 and won't go below 50 mV instead of the desired 0V, causing a non-linearity in the sensor reading. When using a 12 bit ADC, and a reference voltage of 5 Volt (having an ADC step size of approximate 1.2 mV), the output saturation results in a loss of the lower 40 quantization levels of the ADCs dynamic range.

Two-Stage, Single Supply True Zero Amplifier

This sensor application produces a DC signal, amplified by a two cascaded op amps, having a single supply. The output voltage of the second op amp is converted to the digital domain. Figure 30 shows the basic setup of this application.

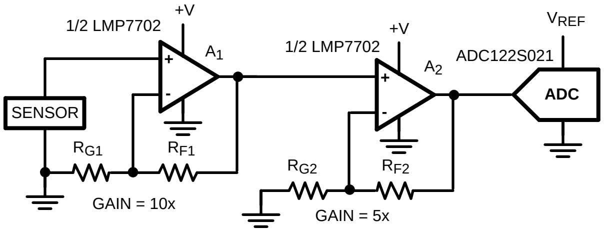


Figure 30. Sensor with DC Output and a 2-Stage, Single Supply Op Amp.

The sensor generates a DC output signal. In this case, a DC coupled, 2-stage amplifier is used. The output voltage swing of the second op amp should me matched to the input voltage range of the Analog to Digital Converter (ADC). For the high side of the range this can be done by adjusting the gain of the op amp. However, the low side of the range can't be adjusted and is affected by the output drive of the op amp.

Example:

Assume; the output voltage range of the sensor is 0 to 90 mV. The available op amp is a LMP7702 (Dual LMP7701 op amp) that can be used for A_1 and A_2. The op amp is using a 0/+5V supply voltage, having an output drive of 50mV from both rails. This results in an output range of 50 mV to 4.95V for each individual amplifier.

Let choose two resistors values for R_{G1} and R_{F1} that result in a gain of 10x for the first stage (A_1) and a gain of 5x for the second stage (A_2) The output of the A_2 in the LMP7702 should swing from 0V to 4.5 Volt. This swing is limited by the 2 different factors:

1. The high voltage swing is no problem; however the low voltage swing is limited by the output saturation voltage of A_2 from the LM7702 and won't go below 50mV instead of the desired 0V.
2. Another effect has more impact. The output saturation voltage of the first stage will cause an offset for the input of the second stage. This offset of A_1 is amplified by the gain of the second stage (10x in this example), resulting in an output offset voltage of 500mV. This is significantly more that the 50 mV (V_{DSAT}) of A_2.

When using a 12 bit ADC, and a reference voltage of 5 Volt (having an ADC step size of approximate 1.2 mV), the output saturation results in a loss of the lower 400 quantization levels of the ADCs dynamic range. This will cause a major non-linearity in the sensor reading.

Dual Supply, True Zero Amplifiers

The limitations of the output stage of the op amp, as indicated in both examples, can be omitted by using a dual supply op amp. The output stage of the used op amp can then still swing from 50 mV of the supply rails. However, the functional output range of the op amp is now from ground level to a value near the positive supply rail. Figure 31 shows the output drive of an amplifier in a true zero output voltage application.

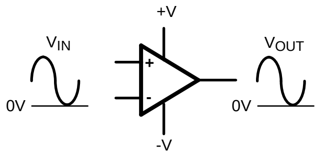


Figure 31. Amplifier output drive with a dual supply

Disadvantages of this solution are:

- The usage of a dual supply instead of a simple single supply is more expensive.
- A dual supply voltage for the op amps requires parts that can handle a larger operating range for the supply voltage. If the op amps used in the current solution can't handle this, a redesign can be required.

A better solution is to use the LM7705. This low noise negative bias generator has some major advantages with respect to a dual supply solution:

- Operates with only a single positive supply, and is therefore a much cheaper solution.
- The LM7705 generates a negative supply voltage of only −0.23V. This is more than enough to create a True-zero output for most op amps.
- In many applications, this "small" extension of the supply voltage range can be within the abs max rating for many op amps, so an expensive redesign is not necessary.

In the next section a typical amplifier application will be evaluated. The performance of an amplifier will be measured in a single supply configuration. The results will be compared with an amplifier using a LM7705 supplying a negative voltage to the bias pin.

TYPICAL AMPLIFIER APPLICATION

This section shows the measurement results of a true zero output amplifier application with an analog to digital converter (ADC) used as back-end. The biasing of the op amp can be done in two ways:

- A single supply configuration
- A single supply in combination with the LM7705, extending the negative supply from ground level to a fixed -0.23 Voltage.

Basic Setup

The basic setup of this true zero output amplifier is given in Figure 32. The LMP7701 op amp is configured as a voltage follower to demonstrate the output limitation, due to the saturation of the output stage. The negative power supply pin of the op amp can be connected to ground level or to the output of the negative bias generator, to demonstrate the V_{DSAT} effect at the output voltage range.

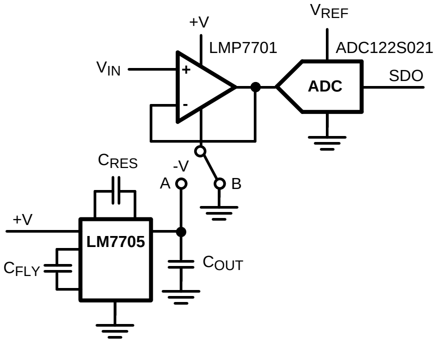


Figure 32. Typical True Zero Output Voltage Application with/without LM7705

The output voltage of the LMP7701 is converted to the digital domain using an ADC122S021. This is an 12 bit analog to digital converter with a serial data output. Data processing and graphical displaying is done with a computer. The negative power supply pin of the op amp can be connected to ground level or to the output of the negative bias generator, to demonstrate the effect at the output voltage range of the op amp.

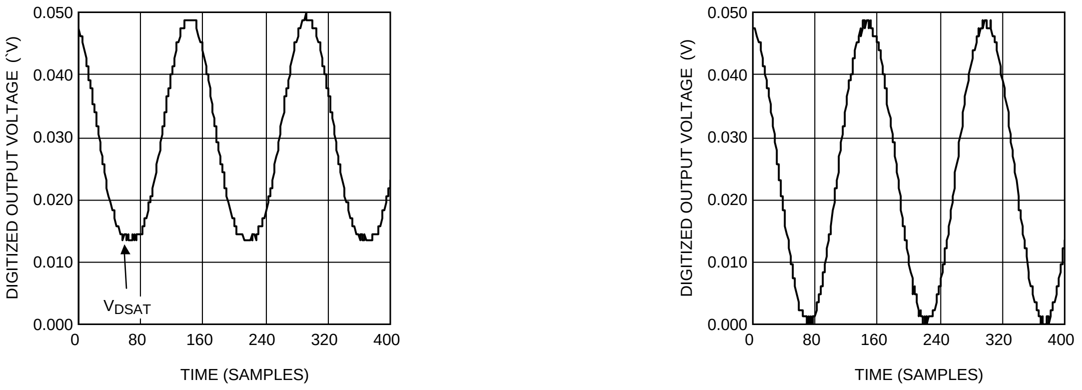
The key specifications of the used components are given in the next part of the section.

Supply Voltage/Reference Voltage	
Supply voltage	+5V
ADC Voltage Reference	+5V
LMP7701	
V_{DSAT} (typical)	18 mV
V_{DSAT} (over temperature)	50 mV
LM7705	
Output voltage ripple	4 mV_{PP}
Output voltage noise	10 mV_{PP}
ADC	
Type	ADC122S021
Resolution	12 bit
Quantization level	5V/4096 = 1.2mV

Measurement Results

The output voltage range of the LMP7701 has been measured, especially the range to ground level. A small DC signal, with a voltage swing of 50 mV_{PP} is applied to the input. The digitized output voltage of the op amp is measured over a given time period, when its negative supply pin is connected to ground level or connected to the output of the LM7705.

Figure 33A and Figure 33B show the digitized output voltage of the LMP7701 op amp.



A B

Figure 33. Digitized Output Voltage without (A) and with (B) LM7705

Figure 33A shows the digitized output voltage of the op amp when its negative supply pin is connected to ground level. The output of the amplifier saturates at a level of 14 mv (this is in line with the typical value of 18 mV given in the datasheet) The graph shows some fluctuations (1 bit quantization error). Figure 33B show the digitized output voltage of the op amp when its negative supply pin is connected to the output of the LM7705. Again, the graph shows some 1 bit quantization errors caused by the voltage ripple and output noise. In this case the op amps output level can reach the true zero output level.

The graphs in Figure 33 show that:

- With a single supply, the output of the amplifier is limited by the V_{DSAT} of the output stage.
- The amplifier can be used as a true zero output using a LM7705.
- The quantization error of the digitized output voltage is caused by the noise and the voltage ripple.
- Using the LM7705 does not increase the quantization error in this set up.

DESIGN RECOMMENDATIONS

The LM7705 is a switched capacitor voltage inverter. This means that charge is transferred from different external capacitors, to generate a negative voltage. For this reason the part is very sensitive for contact resistance between the package and external capacitors. It's also recommended to use low ESR capacitors for C_{FLY}, C_{RES} and C_{OUT} in combination with short traces.

To prevent large variations at the V_{DD} pin of the package it is recommended to add a decouple capacitor as close to the pin as possible.

The output voltage noise can be suppressed using a small RF capacitor, will a value of e.g. 100 nF.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	**Page**
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM7705MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F26A	Samples
LM7705MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F26A	Samples
LM7705MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	F26A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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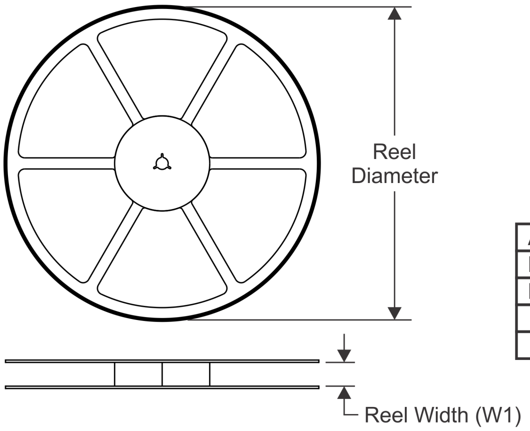
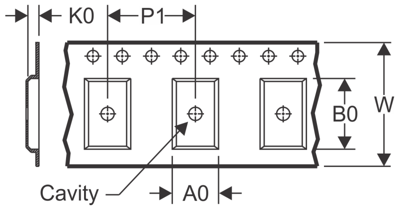
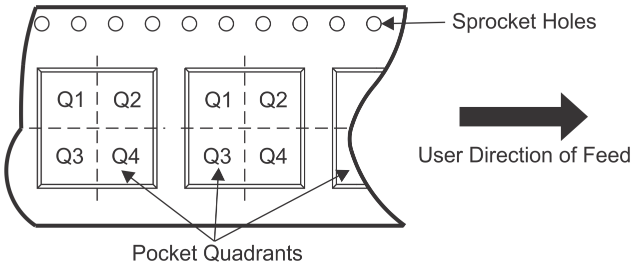


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

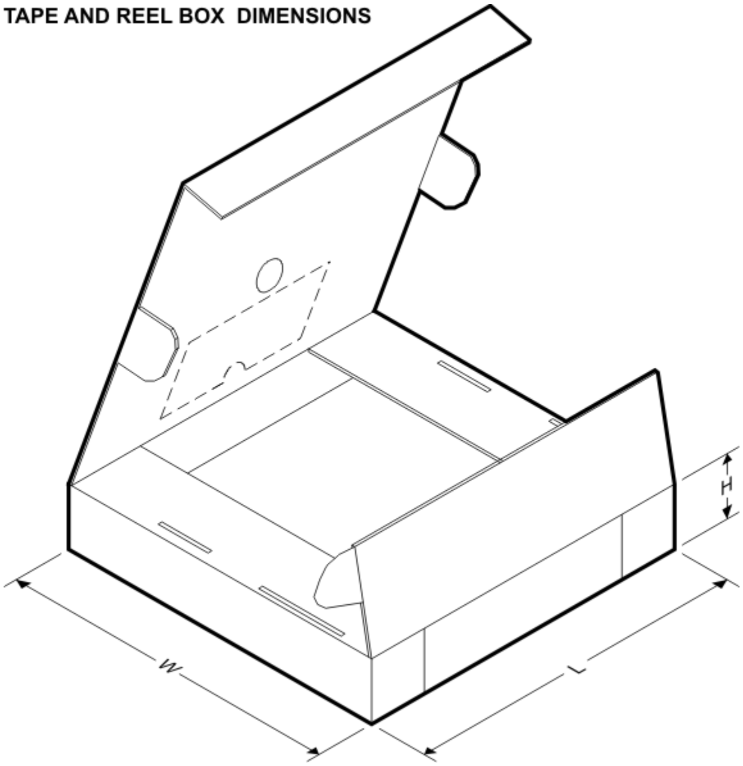
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7705MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7705MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7705MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

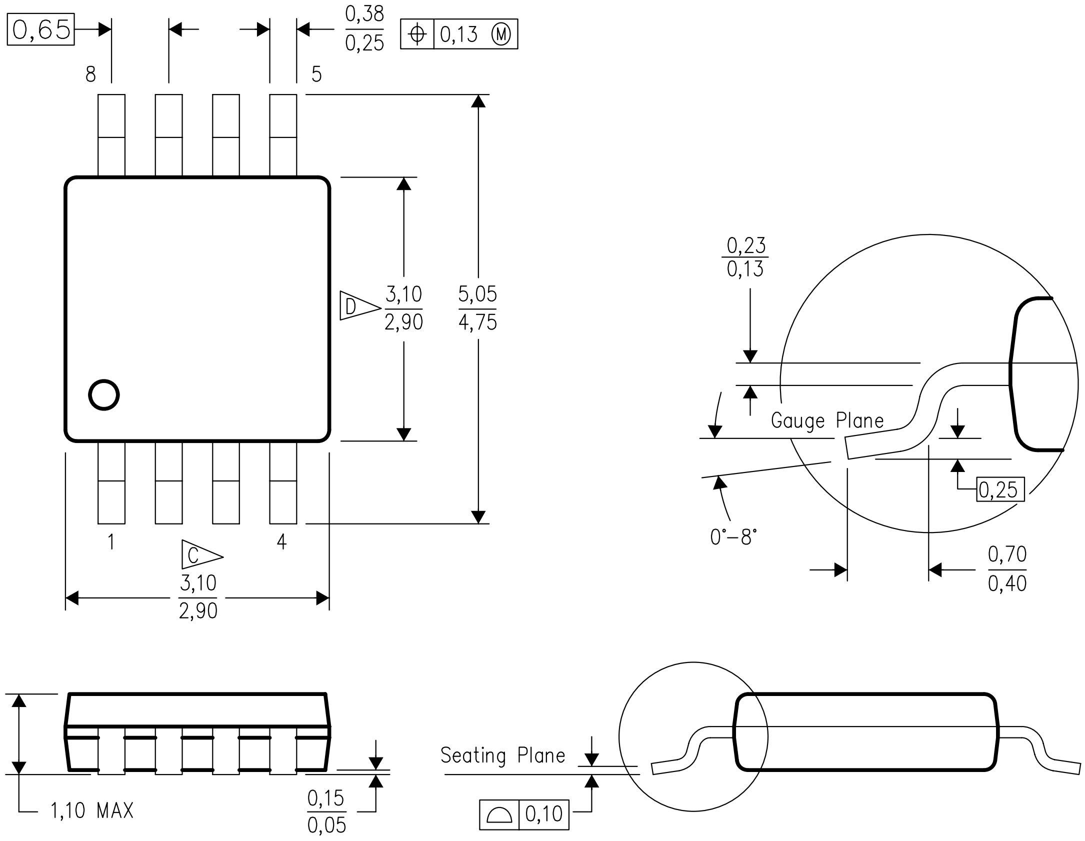
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7705MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM7705MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LM7705MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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